## EXPRESS MAIL LABEL NO. EV 306258357 US ATTORNEY DOCKET NO. N1085-00026 [TSMC2002-0698]

## What is claimed is:

1	1.	A device to control	a sense	amplifier	comprising
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- a resetable control circuit containing a first input, a second input, a third input, and an
- 3 output; said first input coupled to said output or to a ground; said second input coupled to receive
- 4 a start signal; said third input coupled to receive output signals of said sense amplifier; and said
- 5 output coupled to said sense amplifier.
- 1 2. The device of claim 1 wherein said first input, said second input, said third input, and
- 2 said output are initially low; when said second input goes high and then goes low again, said
- 3 output goes high; when said third input goes high, said output goes low.
- 1 3. The device of claim 1 further comprising:
- a reset signal generator, containing a first input coupled to an OUT end of said sense
- 3 amplifier, a second input coupled to an OUTB end of said sense amplifier, and an output coupled
- 4 to said third input of said resetable control circuit; and
- when either OUT or OUTB reaches a predetermined low voltage level, said output of
- 6 said reset signal generator goes high.
- 1 4. The device of claim 1 wherein said resetable control circuit is a flip-flop circuit
- 1 5. The device of claim 4 wherein said flip-flop circuit is a D flip-flop circuit.
- 1 6. The device of claim 5 wherein said first input is a data signal for said D flip-flop circuit.
- 1 7. The device of claim 5 wherein said start signal is a triggered clock for said D flip-flop
- 2 circuit.
- 1 8. The device of claim 7 wherein said start signal is a pseudo word line signal.
- 1 9. The device of claim 5 wherein said third input is a reset signal for said D flip-flop circuit.

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I	10. The device of claim 5 wherein said first input being a data signal for said D flip-flop, said
2	second input being a triggered clock for said D flip-flop, said third input being a reset signal for
3	said D flip-flop, and said output are initially low; when said triggered clock goes high and then
4	goes low again, said output goes high; when said reset signal goes high, said output goes low.
1	11. The device of claim 5 wherein said resetable control circuit further comprises a first
2	passgate, a second passgate, a third passgate, and fourth passgate; a first inverter, a second
3	inverter, a third inverter, a fourth inverter, a fifth inverter, and a sixth inverter; and a first NAND
4	gate;
5	said first input of said resetable control circuit is coupled to an input end of said first
6	passgate, an output end of said first passgate is coupled to an output end of said second passgate
7	and an input end of said third inverter;
8	said second input of said resetable control circuit is coupled to an input end of said first
9	inverter; a C end of said first passgate, a CB end of said second passgate, a CB end of said third
10	passgate, and a C end of said fourth passgate;
11	said third input of said resetable control circuit is coupled to an input end of said second
12	inverter;
13	an output end of said first inverter is coupled to a CB end of said first passgate, a C end
14	of said second passgate, a C end of said third passgate, and a CB end of said fourth passgate;
15	an output end of said third inverter is coupled to a first input end of said first NAND gate
16	and to an input end of said third passgate;
17	an output end of said second inverter is coupled to a second input end of said first NAND
18	gate, an output end of said first NAND is coupled to an input end of said second passgate;
19	an output end of said third passgate is coupled to an input end of said fourth inverter and
20	to an output end of said fourth passgate;
21	an output end of said fourth inverter is coupled to an input end of said fifth inverter and to
22	an input end of said sixth inverter;
23	an output end of said fifth inverter is coupled to an input end of said fourth passgate;
24	an output end of said sixth inverter is coupled to said output of said resetable control
25	circuit.

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l	12.	The device of	claim 11.	further	comprising
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- 2 a reset signal generator, containing a NAND gate, a first input of said NAND gate, a
- 3 second input of said NAND gate, an output of said NAND gate;
- 4 said first input coupled to an OUT end of said sense amplifier, said second input coupled
- 5 to an OUTB end of said sense amplifier, and said output coupled to said third input of said
- 6 resetable control circuit.

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